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FIG. 3F illustrates the fifth embodiment of MCM package structure in the present invention which includes a bare chip and a CSP 373 package with a central pad bonding. The MCM package includes a substrate 31, solder balls 33 under the substrate 31, package mold resin 34, the CSP 373 with a central pad bonding is electrically connected to the substrate 31 by the wires 35, and the bare chip 321 is electrically connected to the substrate 31 by the wires 35.

CLAIMS:

Cancel claims 1-26 and add new claims 41-57 as follows:

41. (New) A multi-chip module package structure comprising:
- a substrate;
 - at least two chip packages, each of said chip packages being a packaged chip module;
 - a plurality of electrical connect points electrically connecting said chip packages with said substrate;
 - a plurality of electrical connect pins; and
 - a package material enclosing said substrate, said connect points and said chip packages.
42. (New) The multi-chip module package structure as claimed in claim 41, wherein each of said chip packages is a chip-scale package or a wafer level chip-scale package.

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1 43. (New) The multi-chip module package structure as claimed in claim 41, wherein at
2 least one of said chip packages is a chip-scale package with wire bonding.

1 44. (New) The multi-chip module package structure as claimed in claim 41, wherein at
2 least one of said chip packages is a chip-scale package with flip chip bonding.

1 45. (New) The multi-chip module package structure as claimed in claim 41, wherein at
2 least one of said chip packages is a chip-scale package with central pad bonding.

1 46. (New) The multi-chip module package structure as claimed in claim 41, wherein said
2 chip packages pass burn-in test and function test.

1 47. (New) The multi-chip module package structure as claimed in claim 41, wherein said
2 plurality of electrical connect pins are solder balls.

1 48. (New) The multi-chip module package structure as claimed in claim 41, wherein said
2 plurality of electrical connect points are solder balls or gold wires.

1 49. (New) A multi-chip module package structure comprising:

2 a substrate;

3 at least a bare chip;

4 at least one chip package, said chip package being a packaged chip module;

5 a plurality of electrical connect points electrically connecting said bare chip and said

6 at least one chip package with said substrate;

7 a plurality of electrical connect pins; and

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8 a package material enclosing said substrate, said connect points, said bare chip and
9 said at least one chip package.

1 50. The multi-chip module package structure as claimed in claim 49, wherein said bare
2 chip is bonded to said substrate by wire bonding or flip chip bonding.

1 51. (New) The multi-chip module package structure as claimed in claim 49, wherein
2 said at least one chip package is a chip-scale package or a wafer level chip-scale
3 package.

1 52. (New) The multi-chip module package structure as claimed in claim 49, wherein
2 said at least one chip package is a chip-scale package with wire bonding.

1 53. (New) The multi-chip module package structure as claimed in claim 49, wherein
2 said at least one chip package is a chip-scale package with flip chip bonding.

1 54. (New) The multi-chip module package structure as claimed in claim 49, wherein
2 said at least one chip package is a chip-scale package with central pad bonding.

1 55. (New) The multi-chip module package structure as claimed in claim 49, wherein
2 said at least one chip package passes burn-in test and function test.

1 56. (New) The multi-chip module package structure as claimed in claim 49, wherein said
2 plurality of electrical connect pins are solder balls.

1 57. (New) The multi-chip module package structure as claimed in claim 49, wherein said
2 plurality of electrical connect points are solder balls or gold wires.